Amendment to Claims

Please amend the claims as shown below and add claims 32-37.

1. (Original) A system comprising:

a processor coupled to memory by a bus, the processor having a processor core and a pad ring, the processor core having an independent power supply;

a voltage regulator providing a plurality of voltages and providing the independent power supply;

a clock signal generator providing a clock signal at a plurality of frequencies;

a state machine to coordinate voltage and clock frequency to the processor core; and

an operating system running on the processor, the operating system monitoring an application mix executing in the processor to determine a required frequency, and determining a minimum voltage at which the processor core can operate at the required frequency, wherein the operating system directs the state machine to enter a state in which the required frequency is supplied by the clock signal generator and a closest supported voltage equal to or greater than the minimum voltage is supplied by the voltage regulator.

2. (Original) The system of claim 1 wherein the voltage regulator provides one of an idle voltage or a peak voltage.

3. (Original) The system of claim 1 wherein the voltage regulator can provide one voltage corresponding to each frequency supported by the clock signal generator.

4. (Original) A method of reducing power consumption by a processor core and a pad ring comprising the steps of:

accepting a measure of processor core performance need of each application

currently seeking access to the processor core;

accumulating each measure of processor core performance need to find total current need:

calculating a minimum frequency that will allow the processor core to meet the total current need for the time period:

selecting a lowest supported frequency equal to or greater than the minimum
frequency to be a required frequency:

finding a minimum supported voltage at which the processor core can operate at the required frequency independent of a voltage required by the pad ring;

supplying the required frequency and the minimum supported voltage to the
processor core; and

dynamically changing the required frequency and the minimum supported voltage supplied responsive to a change in the current application mix.

5. (Original) A method of reducing power consumption by a processor core and a pad ring comprising the steps of:

establishing a maximum allowable power consumption;

finding a maximum supported frequency which will allow the processor core to remain below the maximum allowable power consumption at the minimum supported voltage;

selecting a required frequency to be less than or equal to the maximum supported frequency:

finding a minimum supported voltage at which the processor core can operate at the required frequency independent of a voltage required by the pad ring:

supplying the required frequency and the minimum supported voltage to the
processor core: and

dynamically changing the required frequency and the minimum supported voltage supplied responsive to a change in the current application mix.

6. (Original) The method of claim 5 wherein a required frequency less than the maximum supported frequency is selected whenever a total processor core performance need of the current application mix can be met by a lower supported frequency

7. (Previously amended) An apparatus, comprising:

a static random access memory;

a processor coupled to the static random access memory;

a voltage regulator adapted to provide at least two voltage potential levels to at least a portion of the processor; and

wherein the voltage potential level provided by the voltage regulator is adapted to be adjusted depending on a frequency corresponding to the operational load of the processor.

8 (Original) The apparatus of claim 7, wherein the voltage regulator is adapted to provide an idle voltage potential level and a peak voltage level.

9. (Original) The apparatus of claim 7, further comprising a state machine adapted to determine the operational load of the processor.

10 (Original) The apparatus of claim 9, wherein the state machine is further adapted to determine a minimum voltage potential level at which the processor can operate.

11 (Original) The apparatus of claim 7, further comprising a clock signal generator adapted to provide a clock signal of at least two frequencies.

12. (Original) A method comprising:

determining an instruction mix of a processor;

determining a frequency at which the processor may operate given the instruction mix; and

determining a voltage potential level corresponding to the frequency; and

providing at least a portion of a processor with the frequency and voltage potential level.

13. (Original) The method of claim 12, further comprising changing the frequency and voltage potential level in response to a change in the instruction mix of the processor.

14. (Cancelled) A method of operating a processor, comprising:

monitoring an application mix executed by a processor; and

adjusting the voltage potential level provided to at least a portion of the processor based on the application mix executed by the processor.

15. (Cancelled) The method of claim 14, further comprising determining an operational frequency based on the instruction mix executed by the processor.

16. (Cancelled) The method of claim 15, further comprising adjusting the operational frequency after adjusting the voltage potential level.

17. (Cancelled) An article comprising: a storage medium having stored thereon instructions, that, when executed by a computing platform, results in:

monitoring an application mix executed by a processor; and

adjusting the voltage potential level provided to at least a portion of the computing platform based on the application mix executed by the computing platform.

18. (Cancelled) The article of claim 17, wherein the instructions, when executed, further result in determining a preferred operational frequency based on the instruction mix executed by the computing platform.

19. (Cancelled) The article of claim 17, wherein the instructions, when executed, further result in computing platform executing the instruction mix at peak performance.

20. (Cancelled) The article of claim 17, wherein the article further comprises a static random access memory device and the computing platform is coupled to the static random access memory.

21. (Cancelled) The article of claim 20, wherein the static random access memory is adapted to store the instructions to be executed by the computing platform.

22. (Cancelled) A method comprising operating a core of a device at a voltage independent of a voltage that operates a pad ring of the device.

23. (Cancelled) The method of claim 22 further including operating the core at a minimum supported voltage and operating the pad ring at a voltage different from the core.

24. (Cancelled) The method of claim 22 further including changing the voltage to the core without changing the voltage to the pad ring.

25. (Cancelled) An apparatus, comprising:

a processor;

a voltage regulator adapted to provide at least two voltage potential levels to at least a portion of the processor; and

wherein the voltage potential level provided by the voltage regulator is adapted to be adjusted depending on the operational load of the processor, and is provided to an electrically common terminal in the processor.

32. (Cancelled) A method comprising:

determining a frequency for an application mix and providing a voltage potential for the frequency.

33. (Cancelled) The method of claim 32, wherein providing a voltage potential includes providing a voltage potential to a core of a processor.

34. (Cancelled) The method of claim 33, where in providing a voltage potential includes providing a different voltage potential to a pad of the processor.

35. (Cancelled) An apparatus comprising:

a state machine adapted to determine a frequency for an application mix, wherein the state machine is further adapted to provide a voltage potential to at least a core of a processor for the frequency.

36. (Cancelled) The apparatus of claim 35, further comprising a voltage regulator to provide the voltage potential level.

37. (Cancelled) The apparatus of claim 35, wherein the processor is adapted to receive a clock signal that is varied in accordance with changes in the application mix of the processor.

38. (Reinstated – formerly claim #14) A method of operating a processor, comprising:

monitoring an application mix executed by a processor; and

adjusting the voltage potential level provided to at least a portion of the processor based on the application mix executed by the processor.

39. (Reinstated – formerly claim #15) The method of claim 14, further comprising determining an operational frequency based on the instruction mix executed by the processor.

40. (Reinstated – formerly claim #16) The method of claim 39, further comprising adjusting the operational frequency after adjusting the voltage potential level.

41. (Reinstated – formerly claim #17) An article comprising: a storage medium having stored thereon instructions, that, when executed by a computing platform, results in:

monitoring an application mix executed by a processor; and

adjusting the voltage potential level provided to at least a portion of the computing platform based on the application mix executed by the computing platform.

42. (Reinstated – formerly claim #18) The article of claim 41, wherein the instructions, when executed, further result in determining a preferred operational frequency based on the instruction mix executed by the computing platform.

43. (Reinstated – formerly claim #19) The article of claim 41, wherein the instructions, when executed, further result in computing platform executing the instruction mix at peak performance.

44. (Reinstated – formerly claim #20) The article of claim 41, wherein the article further comprises a static random access memory device and the computing platform is coupled to the static random access memory.

45. (Reinstated – formerly claim #21) The article of claim 44, wherein the static random access memory is adapted to store the instructions to be executed by the computing platform.

46. (Reinstated – formerly claim #22) A method comprising operating a core of a device at a voltage independent of a voltage that operates a pad ring of the device.

47. (Reinstated – formerly claim #23) The method of claim 46 further including operating the core at a minimum supported voltage and operating the pad ring at a voltage different from the core.

48. (Reinstated – formerly claim #24) The method of claim 46 further including changing the voltage to the core without changing the voltage to the pad ring.

49. (Reinstated – formerly claim #25) An apparatus, comprising:

a processor;

a voltage regulator adapted to provide at least two voltage potential levels to at least a portion of the processor; and

wherein the voltage potential level provided by the voltage regulator is adapted to be adjusted depending on the operational load of the processor, and is provided to an electrically common terminal in the processor.

50. (Reinstated – formerly claim #26) The apparatus of claim 49, wherein the voltage regulator is further adapted to provide the voltage potential level depending on an operational frequency of the processor.

51. (Reinstated – formerly claim #27) The apparatus of claim 49, further comprising a state machine responsive to an operational load of the processor.

52. (Reinstated – formerly claim #28) The apparatus of claim 49, wherein said processor is adapted to receive a clock signal that is varied in accordance with changes in the operational load of said processor.

53. (Reinstated – formerly claim #52) A method comprising operating a processor core at a first voltage independent of a second voltage that operates a pad ring associated with the processor core, said first voltage being varied in accordance with changes in an operational load of said processor core.

54. (Reinstated – formerly claim #30) The method of claim 53 further including operating the processor core at a minimum supported voltage and operating the pad ring at a voltage different from the processor core.

55. (Reinstated – formerly claim #31) The method of claim 53 further including changing the first voltage to the processor core without changing the second voltage to the pad ring.

56. (Reinstated – formerly claim #32) A method comprising:

determining a frequency for an application mix and providing a voltage potential for the frequency.

57. (Reinstated – formerly claim #33) The method of claim 56, wherein providing a voltage potential includes providing a voltage potential to a core of a processor.

58. (Reinstated – formerly claim #34) The method of claim 57, where in providing a voltage potential includes providing a different voltage potential to a pad of the processor.

59. (Reinstated – formerly claim #35) An apparatus comprising:

a state machine adapted to determine a frequency for an application mix, wherein the state machine is further adapted to provide a voltage potential to at least a core of a processor for the frequency.

60. (Reinstated – formerly claim #36) The apparatus of claim 59, further comprising a voltage regulator to provide the voltage potential level.

61. (Reinstated – formerly claim #37) The apparatus of claim 59, wherein the processor is adapted to receive a clock signal that is varied in accordance with changes in the application mix of the processor.